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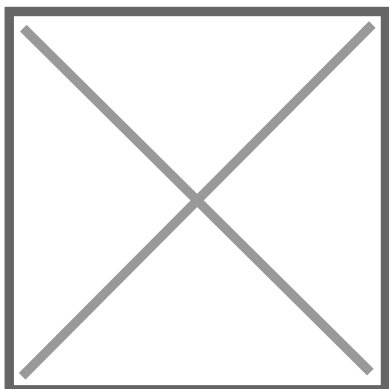
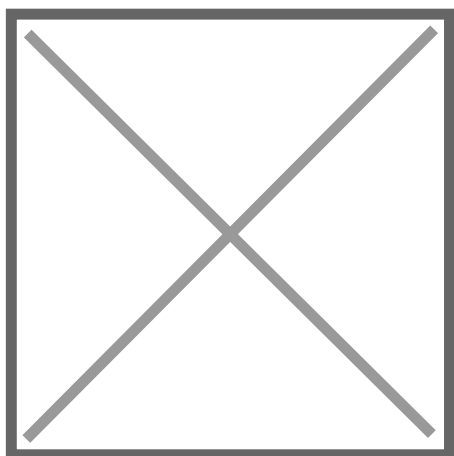
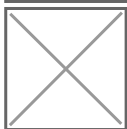
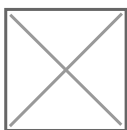
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M2 Integration Circuits Systems



Master's degree

Specialisation Electrical Engineering

Language(s) of instruction

English

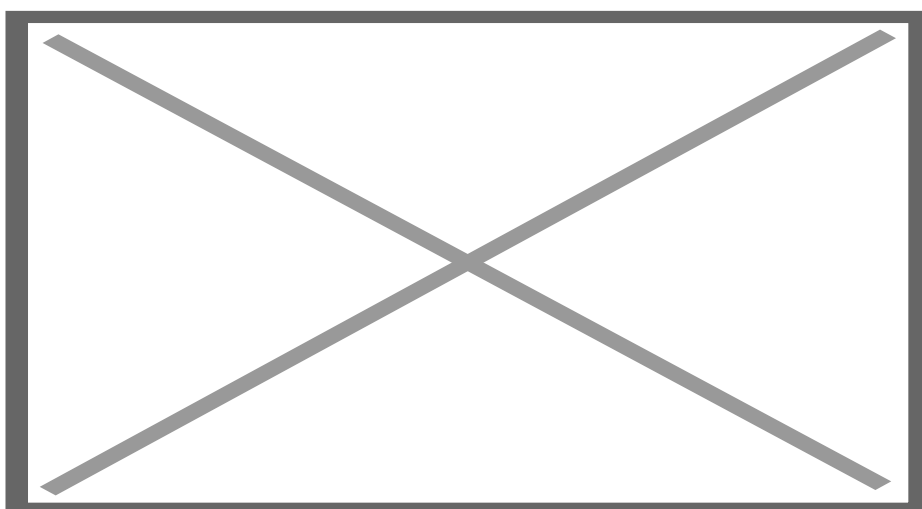
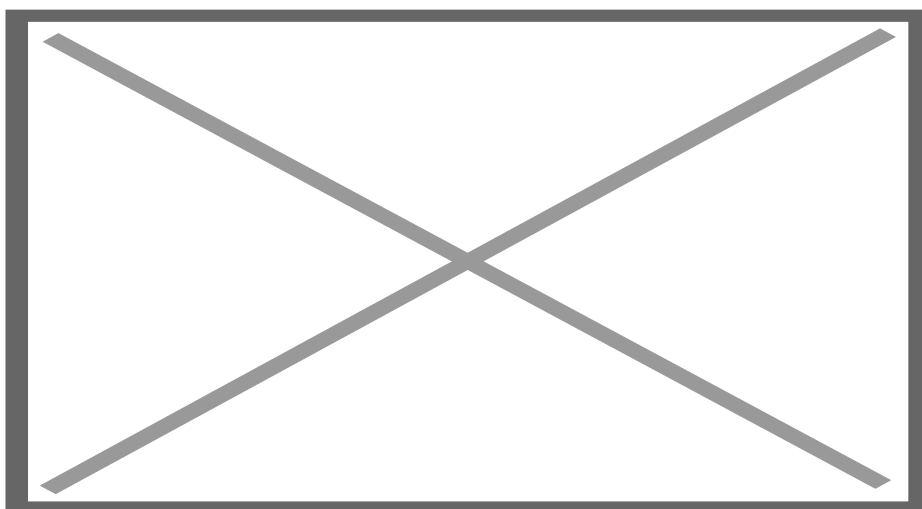
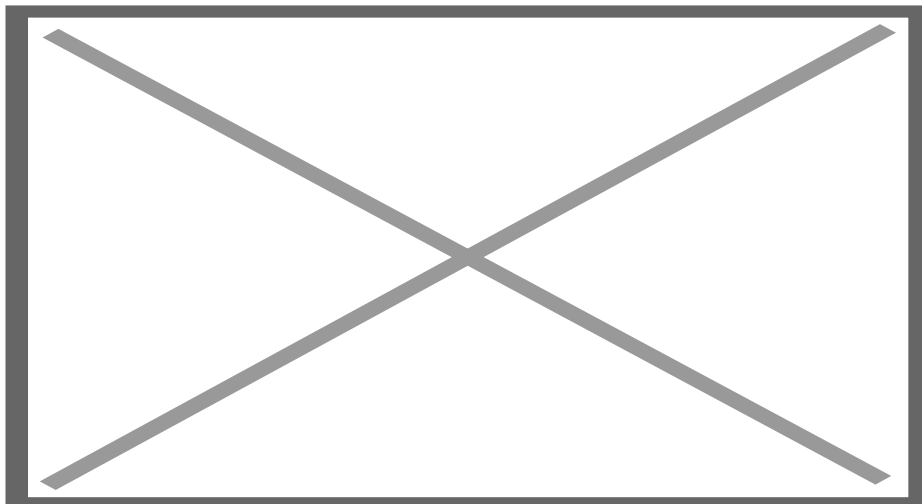
The Integration Circuits and Systems M2 is a curriculum in electronic design. It is jointly run by three leading institutions in the field of electronic design: CentraleSupélec, TelecomParisTech, and Paris-Saclay

University.

The M2 program is structured around courses (from September to March) that focus on projects and practical work (giving students firsthand experience with a range of professional analog and digital CAD tools), followed by an internship period (starting in early April).

[Télécharger la fiche détaillée](#)

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Information

- [Overview](#)
- [Application requirements](#)
- [Schedule](#)

Présentation

Skills

Integrated electronic circuit and system design

Objectives

The objective of the M2 “Integration Circuits and Systems” is to train future researchers or engineers with extensive knowledge and skills in advanced domains of electronic design: analog/digital CAD of microelectronics, analog/digital embedded systems, components and systems for telecommunications, AD/DA conversion, hardware signal processing, sensor interfaces, MEMS, etc.

Calendar

Start of programme (indicative date)

31/08/2026

End of programme (indicative date)

28/09/2027

Admission

Capacity

Available Places

15

Target Audience and Entry Requirements

M1-level students with advanced training in analog and digital electronics.

Période(s) de candidature

Inception Platform

From 02/02/2026 to 21/06/2026

Supporting documents

Compulsory supporting documents

Rank of previous year and size of the promotion.

Motivation letter.

All transcripts of the years / semesters validated since the high school diploma at the date of application.

Certificate of English level.

Certificate of English level (compulsory for non-English speakers).

Mandatory if English not native language

Curriculum Vitae.

Detailed description and hourly volume of courses taken since the beginning of the university program.

Details of the UEs taken for candidates outside the M1 Paris Saclay.

Additional supporting documents

VAP file (obligatory for all persons requesting a valuation of the assets to enter the diploma).

Document indicating the list of local M2 choices available here : <https://urlz.fr/i3Lo>.

Supporting documents :

- Residence permit stating the country of residence of the first country
- Or receipt of request stating the country of first asylum
- Or document from the UNHCR granting refugee status
- Or receipt of refugee status request delivered in France
- Or residence permit stating the refugee status delivered in France
- Or document stating subsidiary protection in France or abroad
- Or document stating temporary protection in France or abroad.

Programme

Second semester

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	practical class	directed study/practical class	distance learning
Internship	24	Semestre 2							
■									

Internship

ECTS : 24

Semester: Semestre 2

Detail

Tutored project 60

Language(s) of instruction

Anglais

Remote teaching

non

Type of assessment

Evaluation Continue non Intégrale

First semester

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	practical class	directed study/practical class
----------	------	----------	---------	----------------	-----------------	------------------------	-----------------	--------------------------------

Circuit nanoarchitecture and deep learning (NARCHI)	3	Semestre 1	16	12
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Circuit nanoarchitecture and deep learning (NARCHI)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 16

Practical study : 12

Language(s) of instruction

Anglais

Remote teaching

non

Type of assessment

Evaluation Continue non Intégrale

[Advanced](#)

[Analog-to-digital](#)

converters and Digital-to-Analog converters (CAN)	3	Semestre 1	9	3	12
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Advanced Analog-to-digital converters and Digital-to-Analog converters (CAN)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 9

Practical study : 12

Directed study: 3

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

M2 level in analog microelectronics equivalent to the "Analog Electronics - Analog Devices and Circuits (EA)" module

Type of assessment

Evaluation Continue non Intégrale

[Mixed-signal,](#)

[Analog & RF](#)

[Systems for](#)

[communicating](#)

[objects](#)

[\(SMART\)](#)

3

Semestre
1

24

0

4.5



Mixed-signal, Analog & RF Systems for communicating objects (SMART)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 24

Practical study : 4.5

Directed study: 0

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

Concepts, architectures and basic components of frontend RF transceiver

Type of assessment

Evaluation Continue non Intégrale

[High](#)

[performance](#)

[sensors and](#)

[transducers](#)

[\(HiPSTR\)](#)

3

Semestre
1

3

21



High performance sensors and transducers (HiPSTR)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 3

Practical study : 21

Language(s) of instruction

Anglais

Remote teaching

non

Type of assessment

Evaluation Continue non Intégrale

[Fundamentals in](#)

[AMS & RF](#)

[Electronics](#)

[\(FARE\)](#)

3

Semestre
1

19.5

0

9



Fundamentals in AMS & RF Electronics (FARE)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 19.5

Practical study : 9

Directed study: 0

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

Basic knowledge in analog electronics : active and passive components, mathematical modeling, Main analog functions: amplifying, filtering, conversion

Type of assessment

Evaluation Continue non Intégrale

[Cell Design For](#)

[Digital](#)

[Integrated](#)

[Circuits](#)

[\(CD2IC\)](#)

3

Semestre
1

12

17



Cell Design For Digital Integrated Circuits (CD2IC)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 12

Practical study : 17

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

M1 level in digital circuits design M1 level in CMOS technology

Type of assessment

Evaluation Continue non Intégrale

CAD of Mixed Integrated Circuit (CAD1)	3	Semestre 1	3	21
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CAD of Mixed Integrated Circuit (CAD1)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 3

Practical study : 21

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

M2 level in Analog integrated circuits equivalent to the "Analog Electronics - Analog Devices and Circuits (EA)" module

Type of assessment

Evaluation Continue non Intégrale

[Algorithms and](#)

[Architectures](#)

[for Digital](#)

[Computing](#)

[\(A2HW\)](#)

3	Semestre 1	21	9	12
---	------------	----	---	----



Algorithms and Architectures for Digital Computing (A2HW)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 21

Practical study : 12

Directed study: 9

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

M2 level in digital circuit design equivalent to the
"Digital Electronics 1 - Digital systems (EN1)"
module

Type of assessment

Evaluation Continue non Intégrale

[Advanced](#)

[Digital](#)

[Electronics](#)

[\(ADE\)](#)

3

Semestre
1

7.5

7.5

9



Advanced Digital Electronics (ADE)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 7.5

Practical study : 9

Directed study: 7.5

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

M1 level in digital circuit design Basic knowledge of
a Hardware description language

Type of assessment

Evaluation Continue non Intégrale

[Advanced](#)

[Design](#)

[Methodologies](#)

[\(CAD2\)](#)



3	Semestre 1	1.5	1.5	27
---	---------------	-----	-----	----

Advanced Design Methodologies (CAD2)

ECTS : 3

Semester: Semestre 1

Detail

Lecture: 1.5

Practical study : 27

Directed study: 1.5

Language(s) of instruction

Anglais

Remote teaching

non

Prerequisites

M2 level in analog microelectronics equivalent to the "Analog Electronics - Analog Devices and Circuits (EA)" module

M2 level in integrated circuits CAD equivalent to the "CAD of Mixed Integrated Circuit (CAD)" module

Type of assessment

Evaluation Continue non Intégrale

[Analog Circuits](#)

[Architectures](#)

[\(ARCHAN\)](#)



3	Annualisé 24	6
---	--------------	---

Analog Circuits Architectures (ARCHAN)

ECTS : 3

Semester: Annualisé

Detail

Lecture: 24

Practical study : 6

Language(s) of instruction

Anglais

Remote teaching

non

Type of assessment

Evaluation Terminale

[Project \(PRJ\)](#)

3	Semestre 2
---	---------------



Project (PRJ)

ECTS : 3

Semester: Semestre 2

Detail

Tutored project 150

Language(s) of instruction

Anglais

Remote teaching

non

Type of assessment

Evaluation Continue non Intégrale

[UE libre](#)

2.5

Semestre

[Catalogue S1](#)

1



UE libre Catalogue S1

ECTS : 2.5

Semester: Semestre 1

Language(s) of instruction

Français

Remote teaching

non

Type of assessment

Evaluation Terminale

Teaching Location(s)

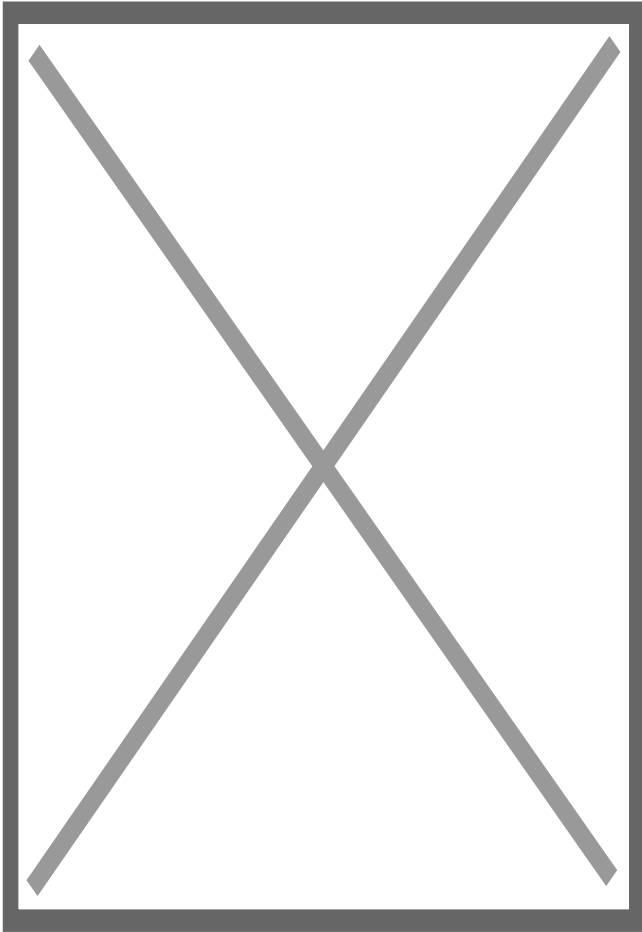
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PALAISEAU

Training campus

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RER B Le guichet

[Voir](#)

Student restaurant (CROUS)

Library

Sports facilities

Student residence

Contact

- **Patricia Desgreys**
Télécom ParisTech
- **Jérôme JUILLARD**
CentraleSupélec
- **CentraleSupélec SUPPORT SCOLARITE**
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<http://www.universite-paris-saclay.fr/formation/master/electronique-energie-electrique-automatique/m2->

