Université Paris-Saclay
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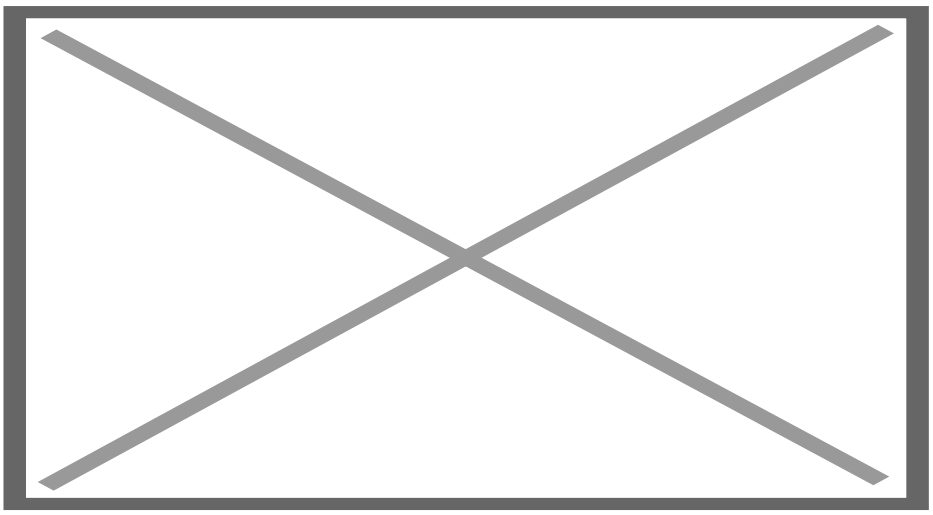
M2 Integration Circuits Systems

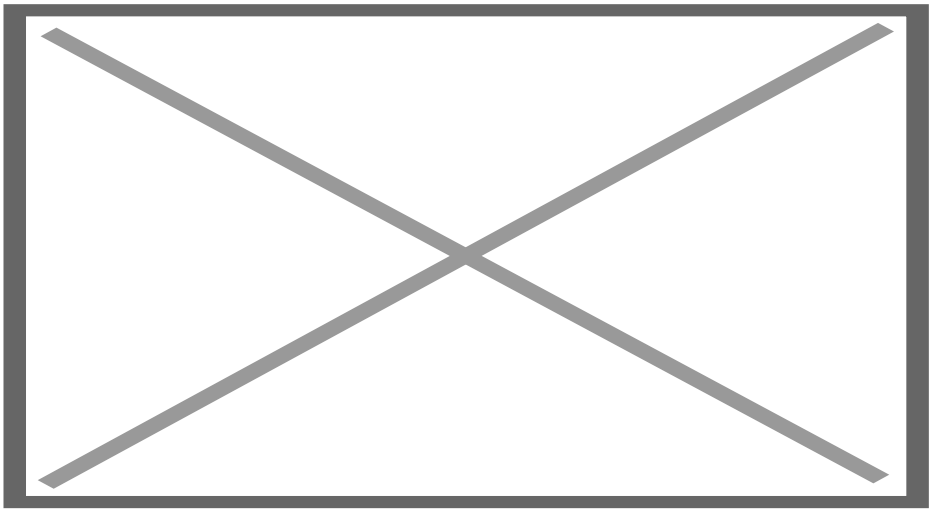
Master's degree
Specialisation Electrical Engineering
Enrolment type
Formation initiale
Formation continue
Language(s) of instruction
English

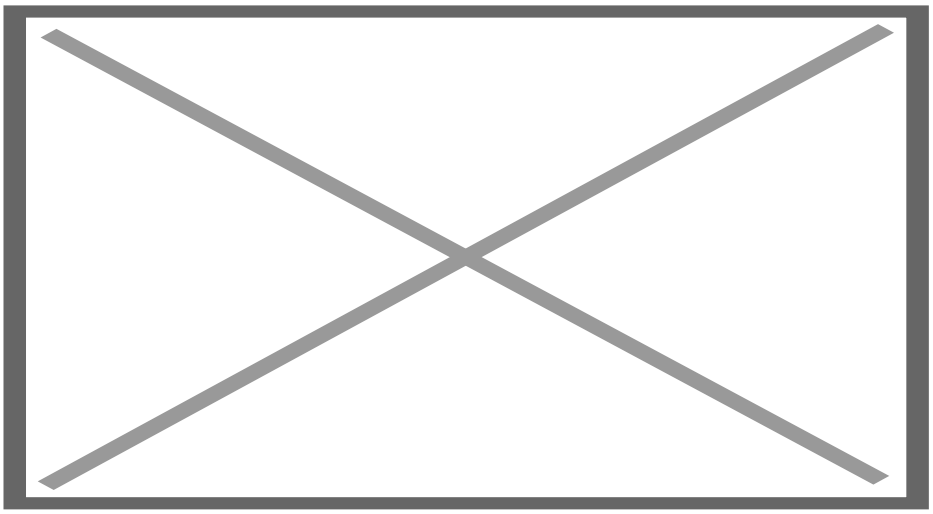
The Integration Circuits and Systems M2 is a curriculum in electronic design. It is jointly run by three leading institutions in the field of electronic design: CentraleSupélec, TelecomParisTech, and Paris-Saclay University.

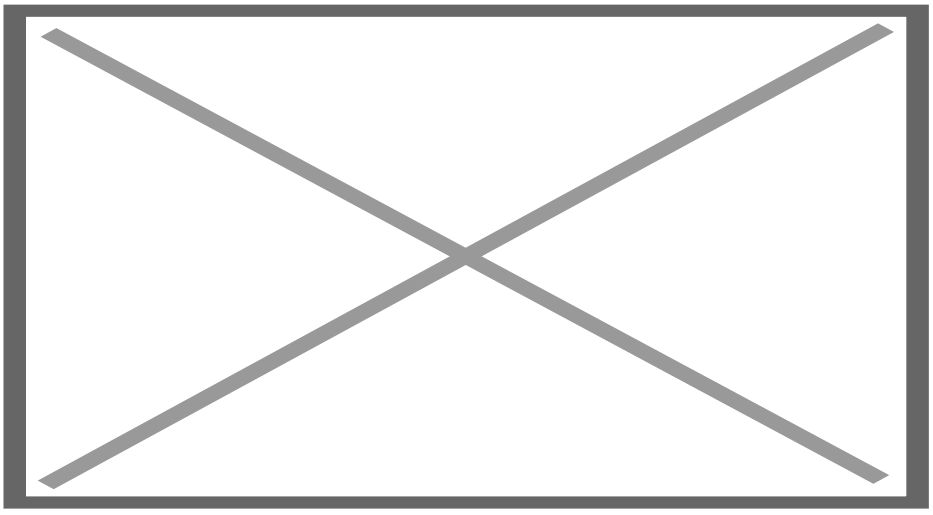
The M2 program is structured around courses (from September to March) that focus on projects and practical work (giving students firsthand experience with a range of professional analog and digital CAD tools), followed by an internship period (starting in early April).

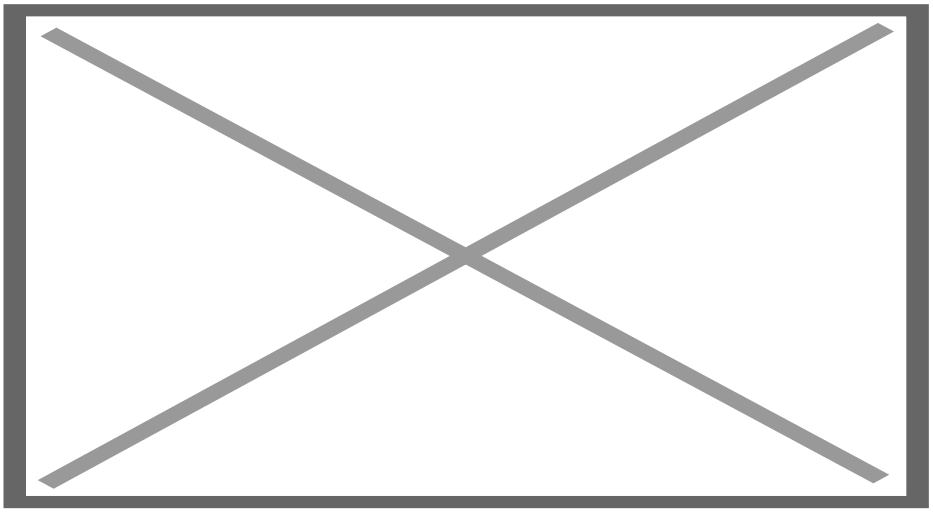
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Information

- Overview
- Application requirements
- Schedule

Présentation

Skills

Integrated electronic circuit and system design

Objectives

The objective of the M2 “Integration Circuits and Systems” is to train future researchers or engineers with extensive knowledge and skills in advanced domains of electronic design: analog/digital CAD of microelectronics, analog/digital embedded systems, components and systems for telecommunications, AD/DA conversion, hardware signal processing, sensor interfaces, MEMS, etc.

Calendar

Start of programme (indicative date)
31/08/2026
End of programme (indicative date)
28/09/2027
Admission

Capacity

Available Places

Target Audience and Entry Requirements

M1-level students with advanced traing in analog and digital electronics.

Période(s) de candidature

Inception Platform

From 02/02/2026 to 21/06/2026

Supporting documents

Compulsory supporting documents

Rank of previous year and size of the promotion.

Motivation letter.

All transcripts of the years / semesters validated since the high school diploma at the date of application.

Certificate of English level.

Certificate of English level (compulsory for non-English speakers).

Mandatory if english not native language

Curriculum Vitae.

Detailed description and hourly volume of courses taken since the beginning of the university program.

Details of the UEs taken for candidates outside the M1 Paris Saclay.

Additional supporting documents

VAP file (obligatory for all persons requesting a valuation of the assets to enter the diploma).

Document indicating the list of local M2 choices available here : https://urlz.fr/i3Lo.

Supporting documents :
- Residence permit stating the country of residence of the first country
- Or receipt of request stating the country of first asylum
- Or document from the UNHCR granting refugee status
- Or receipt of refugee status request delivered in France
- Or residence permit stating the refugee status delivered in France
- Or document stating subsidiary protection in France or abroad
- Or document stating temporary protection in France or abroad.

Programme

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	Lecture/practical class	directed study/practical class	distan learn cour
Internship	24	Semestre 2							

Charger le détail

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	Lecture/practical class	directed study/practic class
Circuit nanoarchitecture and deep learning (NARCHI)	3	Semestre 1	16		12			

Charger le détail

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	Lecture/practical class	directed study/practic class
Advanced Analog-to-digital converters and Digital-to-Analog converters (CAN)	3	Semestre 1	9	3	12			

Charger le détail

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	Lecture/practical class	directed study/practic class
Mixed-signal, Analog & RF Systems for communicating objects (SMART)	3	Semestre 1	24	0	4.5			

Charger le détail

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	Lecture/practical class	directed study/practic class
High performance sensors and transducers (HiPSTR)	3	Semestre 1	3		21			

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed	Lecture/practical	directed study/practic class
Charger le détail Fundamentals in AMS & RF Electronics (FARE)	3	Semestre 1	19.5	0	9			
Charger le détail Cell Design For Digital Integrated Circuits (CD2IC)	3	Semestre 1	12		17			
Charger le détail CAD of Mixed Integrated Circuit (CAD1)	3	Semestre 1	3		21			
Charger le détail Algorithms and Architectures for Digital Computing (A2HW)	3	Semestre 1	21	9	12			
Charger le détail Advanced Digital Electronics (ADE)	3	Semestre 1	7.5	7.5	9			
Charger le détail Advanced Design Methodologies (CAD2)	3	Semestre 1	1.5	1.5	27			
Charger le détail Analog Circuits Architectures (ARCHAN)	3	Annualized	24		6			
Charger le détail Project (PRJ)	3	Semestre 2						
Charger le détail								

Subjects	ECTS	Semester	Lecture	directed study	practical class	Lecture/directed study	Lecture/practical class	directed study/practic class
UE libre Catalogue S1	2.5	Semestre 1						

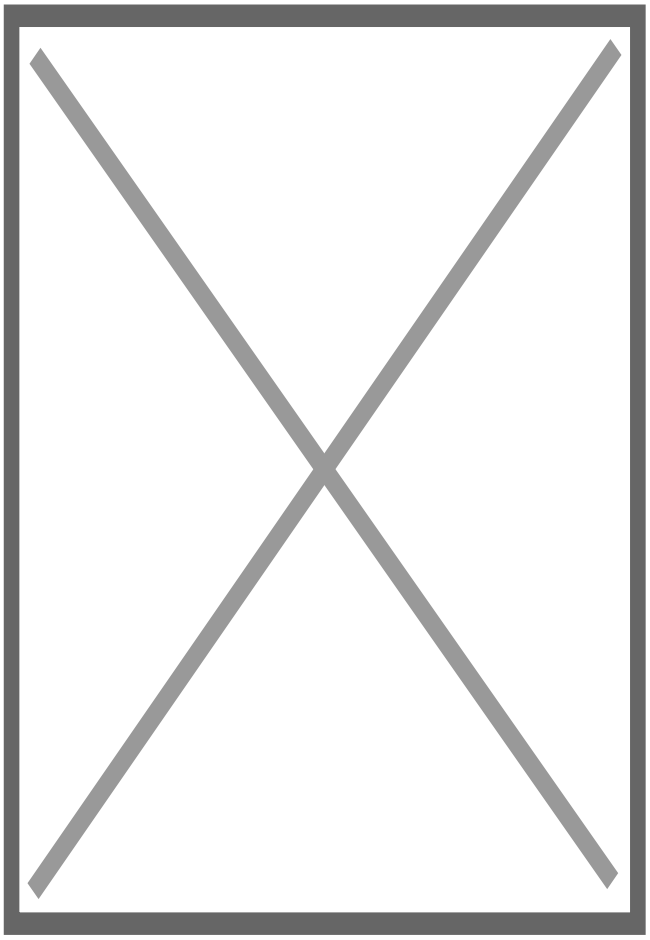
Charger le détail

Teaching Location(s)

ORSAY
GIF SUR YVETTE
PALAISEAU

Training campus

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Saclay Moulon

Saclay / Gif-sur-Yvette / Orsay
Bus 4606 / 4609 / 4611 / 5154
RER B Le guichet
Voir
Student restaurant (CROUS)
Library
Sports facilities
Student residence

Contact

- **Patricia Desgreys**

  Télécom ParisTech
- **Jérôme JUILLARD**

  CentraleSupélec
- **CentraleSupélec SUPPORT SCOLARITE**

  Support scolarité

integration-circuits-systemes